Amendment to the Specification

Please replace the paragraph beginning on page 24 at li 14 with the following amended paragraph:

The clock signal is required to ensure that the ~~opposed~~ opposite transmitter and receiver sections 9 and 10 in the switches 3 at each end of each communications link in the system are sending and receiving data at the same rate in order to allow reliable transmission of data.

Please replace the paragraph beginning on page 24 at li 20 with the following amended paragraph:

In the inventive electronic network architecture, the opposite ~~the opposed~~ transmitter and receiver pairs 9 and 10 in the switches 3 of adjacent nodes are connected so as to form an asynchronous logic loop which generates a clock sign used to synchronize the transmitters and receivers and the data link between them. This logic loop is shown diagrammatically in Figure 10.